Amendments to the Claims:

1. (Currently Amended) A computer implemented method of modeling the static timing behavior a combinatorial gate comprising:

determining that a data signal has been propagated to a first input of the combinatorial gate;

determining that a clock signal has been propagated to a second input of the combinatorial gate;

determining that an output signal of the combinatorial gate has been propagated to an evaluate node of a dynamic circuit;

labeling the combinatorial gate as a near dynamic circuit; and

propagating the output signal of the combinatorial gate as a dynamic signal.

~~propagating the clock signal as an output signal of the combinatorial gate when the output of the combinatorial gate feeds into a clock input of a sequential circuit;~~

~~propagating the data signal as an output signal of the combinatorial gate when the output of the combinatorial gate feeds into a data input of a dynamic circuit; and~~

~~providing a static timing model of the combinatorial gate.~~

2. (Previously Presented) The method of claim 1 further comprising:

performing a reverse traversal function on a circuit design containing the combinatorial gate.

3. (Currently Amended) The method of claim 1 wherein:

propagating the [[data]] output signal includes causing a later arriving edge of the data signal to cause the output signal to respond.

4. (Currently Amended) The method of claim 1 wherein:

the data signal includes a single edge per clock period~~; and,~~

~~when propagating the data signal, the single edge~~ that is propagated through the combinatorial gate.

5. (Cancelled)

6. (Currently Amended) A computer implemented method of classifying a combinatorial gate where the combinatorial gate receives a data signal and a clock signal comprising:

determining that an output of the combinatorial gate is tied to one of an evaluate node of a dynamic circuit, a clock input of a sequential circuit, and a data input of a sequential circuit;

performing a reverse traversal function on a circuit containing the combinatorial gate;

classifying the combinatorial gate as a clock gate when the output of the combinatorial gate is tied to a clock input of a sequential circuit;

classifying the combinatorial gate as a combinatorial gate when the output of the combinatorial gate is tied to a data input of a sequential circuit; and

classifying the combinatorial gate as a near domino gate when the output of the combinatorial gate is tied to a data input of a dynamic circuit.

7. (Cancelled)

8. (Currently Amended) The method of claim [[7]] 6 wherein:

classifying the combinatorial gate as a near domino gate further comprises causing a later arriving edge of the data signal to cause the output signal to respond.

9. (Currently Amended) The method of claim [[7]] 6 wherein:

the data signal includes a single edge per clock period; and,

when classifying the combinatorial gate as a near domino gate, the single edge is propagated through the combinatorial gate.

10. (Currently Amended) The method of claim [[7]] 6 wherein:

the clock signal includes two edges per clock period; and,

when classifying the combinatorial gate as a clock gate, the two edges are propagated through the combinatorial gate.

11-15. (Cancelled)

16. (Currently Amended) A computer based static timing engine comprising:

a data model, the data model including a combinational block determinator module, the combinational block determinator module including means for performing a reverse traversal function on a circuit containing [[the]] a combinatorial gate where the combinatorial gate receives a data signal and a clock signal, and

a timing engine portion coupled to the data model, the timing engine portion including

means for determining that an output of the combinatorial gate is tied to one of a clock input node and an evaluate node of a dynamic circuit;

means for modeling an output of the combinatorial gate as a clock signal when an input to a next element of the circuit is clock input; and,

means for modeling the output of the combinatorial gate as a [[data]] dynamic signal when an input to a next element of the circuit is ~~a data input~~ an evaluate node of a dynamic circuit.

17. (Currently Amended) The static timing engine of claim 16 wherein:

the means for modeling the output of the combinatorial gate as a [[data]] dynamic signal includes means for modeling a near domino gate.

18. (Previously Presented) The static timing engine of claim 17 wherein:

the near domino gate includes causing a later arriving edge of the data signal to cause the output signal to respond.

19. (Previously Presented) The static timing engine of claim 17 wherein:

the data signal includes a single edge per clock period; and,

when providing the near domino gate, the single edge is propagated through the combinatorial gate.

20. (Original) The static timing engine of claim 17 wherein:

the clock signal includes two edges per clock period; and,

when propagating the clock signal, the two edges are propagated through the combinatorial gate.